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EXAMINER	
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ART UNIT	PAPER NUMBER
2871	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/082,984	KONISHI ET AL.	
	Examiner	Art Unit	
	ANDREW SCHECHTER	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 7-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 7-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 23 February 2009 have been fully considered but they are not persuasive.

The applicant argues [pp. 4-5] that *Lee* does not teach that the second metallic line is formed in a side where the TFT array substrate is cut off or chamfered off. This is not persuasive. The second metallic line [24a] in *Song* is formed in the region of the substrate at which the gate pad is formed, as the applicant agrees [see p. 4], and *Lee* discloses and teaches cutting off the substrate on the side of the TFT array substrate at which the gate pad is formed [along cutting line 11, which is along the side with the gate pads, and also happens to be along the side of the substrate with the data pads], as set forth in the rejection.

The applicant refers to the dummy gate line [111] in Fig. 14 of *Lee* and argues that this is not formed where the TFT substrate is cut off, so that the dummy gate line [111] cannot be the second metallic line of claim 1. This is not a persuasive argument for patentability. First, the rejection does not call for the dummy gate line to be the second metallic line of claim 1; the rejection never mentions the dummy gate line [111] of *Lee* and clearly states that element [24a] of *Song* corresponds to the second metallic line of claim 1. Second, *Lee* is only relied upon to teach cutting off the edges of the substrate [which have shorting bars] during the manufacturing process, not to teach anything related to the dummy gate lines. Third, it appears that the applicant may have

misinterpreted the examiner's suggestion that Fig. 14 of *Lee* should be compared to Fig. 12 of *Song*, for instance, in order to see that the devices were analogous; the examiner did not mean to suggest that the function of the specific structures in these figures was identical, only that the common layer structure showed that the devices were analogous: substrate, gate wiring layer, gate insulating layer, semiconductor layer, source/drain layer, passivation layer, ITO layer, and so on. *Lee* is mostly concerned with the structure at the periphery of the display, so it does not appear to have a figure corresponding exactly to the pixel structure in area "C" of *Song's* Fig. 12; the closest in terms of function might be the dummy pixel structure in Figs. 17 and 18, which has of course almost the identical structure to area "C" in *Song's* Fig. 12 (though it is for a dummy pixel electrode rather than a "real" pixel electrode). In any case, the rejection does not mean to rely upon the specific structure in *Lee's* Fig. 14, but only on *Lee's* teaching of the shorting bar and cutting line, which are clearly shown in Fig. 3.

The previous rejections are therefore maintained, modified as necessary by the amendments to the claims.

Claim Objections

2. Claim 1 is objected to because of the following informalities: in the 2nd to last line, "is cut off" should be "which is cut off" and "said both gate insulating film and said passivation film" should be "both said insulating layer and said passivation film" since the insulating layer is not referred to as a gate insulating film in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Song et al.,* U.S. Patent No. 5,851,918 in view of *Takizawa et al.,* U.S. Patent No. 5,742,074 and further in view of *Lee et al.,* U.S. Patent No. 6,587,160.

Song discloses [see Fig. 12, for instance] a TFT array substrate [22, etc.], comprising a display area ["C"] including a pixel electrode [40 in the "C" region], a switching element [24, 30, 34, etc.] connected to the pixel electrode, and a terminal (region) ["D"] formed outside the display area, wherein the terminal comprises a terminal electrode [40 in the "D" region], and a first metallic line [34c, made of chromium, col. 5, lines 43-44] and a second metallic line [24a, made of aluminum, col. 5, lines 18-19], arranged beneath the terminal electrode, and each are connected to the terminal electrode via a contact hole [the holes in passivation layer 36], wherein the first metallic line is formed in a side of the display area, wherein the TFT array further comprises an insulating layer [28] which is interposed between the first metallic line and the second metallic line [note that, as shown in the applicant's own Figs. 2 and 3, the first and second metallic lines do not need to overlap each other in order for the insulating layer to be "interposed between" them]; wherein the first metallic line is formed over the

insulating layer; wherein the second metallic line is formed beneath the insulating layer; wherein any one of the first metallic line and the second metallic line [in this case the first metallic line 34c] is formed in the same layer of the source line [the layer of 34a and 34b], and the other one of the two metallic lines [in this case the second metallic line 24a] is formed in the same layer of the gate line [the layer of 24]; wherein said first and second metallic lines are connected [to each other] via a contact hole [the contact hole in the passivation layer at the far right of the figure, for instance] formed in a passivation film [36] which is provided beneath the terminal electrode; and wherein said second metallic line [which is to be formed in the side of the TFT array substrate which is cut off or chamfered off, as discussed below] is formed beneath both said insulating layer [28] and said passivation film [36].

Song is silent on, and therefore does not explicitly disclose, the following conventional details of TFT arrays for LCDs: a gate line connected to the switching element and a source line connected to the switching element; and the terminal being for connecting the gate line and source line to wirings from an external signal source, with the terminal electrode connected to wirings from the external signal source. *Takizawa* discloses an analogous LCD, with analogous display and terminal areas [see Fig. 1 or 24, for instance], and explicitly discloses a gate line [14] connected to the analogous switching element [40] and a source line [16] connected to the switching element [see Fig. 3, for instance]; and the terminal being for connecting the gate line and source line to at least one external signal source, with the terminal electrode connected to wirings from the external signal source [see col. 7, lines 25-30, for

instance]. It would have been obvious to one of ordinary skill in the art to have these conventional features in the device of *Song*, motivated by the desire to form a functioning LCD with an active matrix of gate and data lines to produce an image from an array of pixels, and to provide the external signals which direct what image is to be formed, respectively.

Song discloses that the first metallic line is formed in a side of the display area, but does not appear to explicitly disclose that the second metallic line is formed in a side where the TFT array substrate is cut off or chamfered off. However, *Lee* discloses [see Figs. 3 and 14, for instance] an analogous device to that of *Song* [compare Fig. 14 to Fig. 12 of *Song*, for instance], in which there is explicitly shown a shorting bar [102] and a cutting line [11] on the other side of the terminals from the display area. It would have been obvious to one of ordinary skill in the art to cut off the substrate during fabrication of *Song's* device as shown in *Lee*, motivated by the desire to have a shorting bar to prevent electrostatic charge damage during the fabrication, and the desire to remove the shorting bar so that the signal lines are not shorted to each other during use, as well as getting rid of excess unused peripheral areas to make the display more compact.

Claim 1 is therefore unpatentable.

Considering claim 7, *Song* does not explicitly disclose that the first metallic line is connected to the source line. However, the purpose of these terminal structures is to be connected to such lines, as can be seen in the analogous LCD shown in Figs. 24-32 of *Takizawa* [this is the fourth embodiment, which discloses, like *Song,* electrodes connected via respective contact holes to two lines below them, see Fig. 28D in

particular]. Considering the source lines and source terminals in Figs. 28D and 32, for instance, the electrodes [35] are analogous to the terminal electrodes [40] in *Song*, being connected through one contact hole to a lower electrode [34b, like the second metallic line in *Song*] and through another contact hole to a slightly higher electrode [36b, like the first metallic line in *Song*], which is connected to the source line [16b]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the first metallic line in *Song* connected to the source line, motivated by the desire to use the terminal structure in *Song* to provide for electrical connection to the source lines. Claim 7 is therefore unpatentable.

Considering claim 8, *Song* does not explicitly disclose that the second metallic line is connected to the gate line. However, the purpose of these terminal structures is to be connected to such lines, as can be seen in the analogous LCD shown in Figs. 24-32 of *Takizawa* [this is the fourth embodiment, which discloses, like *Song,* electrodes connected via respective contact holes to two lines below them, see Fig. 28D in particular]. Considering the gate lines and gate terminals in Figs. 28D and 32, for instance, the electrodes [25] are analogous to the terminal electrodes [40] in *Song*, being connected through one contact hole to a lower electrode [24a, like the first metallic line in *Song*] and through another contact hole to an even lower electrode [26a, like the second metallic line in *Song*], which is connected to the gate line [14a]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the first metallic line in *Song* connected to the gate line, motivated by

the desire to use the terminal structure in *Song* to provide for electrical connection to the gate lines. Claim 8 is therefore unpatentable.

Note that in claim 7 the recited terminal electrode is connected to a source line, and in claim 8 the recited terminal electrode is connected to a gate line. The rejection above should therefore be understood to refer to two separate terminal electrodes in the device of *Song* in view of *Takizawa*, one on the source side of the display for claim 7, and one on the gate side of the display for claim 8, rather than a single terminal electrode satisfying both claims.

The device is a display device, so claims 9-11 are also unpatentable.

The first metallic line and the second metallic line are connected via a plurality of contact holes [the one already discussed at the far right of *Song's* Fig. 12 and the one where element 38 is located]. Claim 12 is therefore unpatentable.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,172,733 to *Hong et al.* discloses [see Fig. 8, for instance] gate pads with multiple contact holes connecting the terminal to an underlying gate bus line, rather than the single such hole *Song* uses to connect the analogous terminal to each of its two underlying metallic lines.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew Schechter/
Primary Examiner, Art Unit 2871
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22 May 2009